IN THE CLAIMS

What is claimed:

1. An apparatus comprising:

a substrate;

a device on the substrate including a gate electrode on a surface of the substrate and a first junction region and a second junction region in the substrate adjacent the gate electrode; and

a silicon alloy material disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate.

2. The apparatus of claim 1, wherein a surface of the substrate defines a top surface of the substrate and the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate.

3. The apparatus of claim 1, wherein the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers.

4. The apparatus of claim 3, wherein the first junction region and the second junction region define a depth in the range of between 30 nanometers and 250 nanometers in depth.

5. The apparatus of claim 1, wherein the substrate is under a strain caused by a silicon alloy lattice spacing of the silicon alloy.

6. The apparatus of claim 1, wherein the silicon alloy material has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material.

7. The apparatus of claim 6, wherein the substrate is under a compressive strain caused by the silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material.

8. The apparatus of claim 1, wherein a surface of the substrate proximate to the first junction region defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region defines a second substrate sidewall surface and the silicon alloy material disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface.

9. The apparatus of claim 1, wherein the silicon alloy material comprises an epitaxial layer of silicon alloy material.

10. The apparatus of claim 1, wherein the silicon alloy material comprises one of silicon germanium (Si_{y-x} Ge_x), silicon carbide (Si_{y-x} C_x), nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

11. The apparatus of claim 1, further comprising a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode, wherein the layer of silicide material comprises one of nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$).

12. The apparatus of claim 11, further comprising a layer of conformal etch stop material on the layer of silicide material, wherein the layer of etch stop material comprises one of silicon dioxide (SiO_2), phosphosilicate glass (PSG, a Phosphorous doped SiO_2), silicon nitride (Si_3N_4), and silicon carbide (SiC).

13. The apparatus of claim 12, further comprising a layer of dielectric material comprising on the layer of conformal etch stop material, wherein the layer of dielectric material comprises one of carbon doped oxide (CDO), cubic boron nitride (CBN), silicon dioxide (SiO_2), phosphosilicate glass (PSG), silicon nitride (Si_3N_4), fluorinated silicate glass (FSG), and silicon carbide (SiC).

14. An apparatus comprising:
a substrate;

a device on the substrate including a gate electrode on a top surface of the substrate and a first junction region and a second junction region in the substrate adjacent the gate electrode; and

a silicon alloy material having a silicon alloy lattice spacing that is different than a lattice spacing of the substrate disposed in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are superior to the top surface of the substrate by a length sufficient to cause a strain in the substrate.

15. The apparatus of claim 14, wherein the substrate comprises an N-type channel/well material of one of silicon, polycrystalline silicon, and single crystal silicon having an electrically negative charge, and wherein the silicon alloy material comprises a P-type junction region material having an electrically positive charge.

16. The apparatus of claim 15, wherein the silicon alloy is silicon germanium having a lattice spacing that is larger than a lattice spacing of the N-type channel/well material, and wherein the strain is a compressive strain.

17. A method comprising:

forming a device on a substrate, the device including:

a gate electrode on a surface of the substrate;

a first junction region and a second junction region in the substrate adjacent the gate electrode; and

depositing a silicon alloy material in each of the first junction region and the second junction region such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface of the substrate.

18. The method of claim 17, wherein depositing the silicon alloy material comprises depositing a sufficient thickness of silicon alloy material having a larger lattice spacing than a lattice spacing of the substrate to cause a compressive strain in the range between 0.5 percent compression and 2.5 percent compression in the substrate.

19. The method of claim 17, wherein depositing the silicon alloy material comprises a chemical vapor deposition sufficient to form an epitaxial layer of silicon alloy material.

20. The method of claim 17, wherein depositing the silicon alloy material comprises depositing silicon alloy material in the first junction region superjacent to a first substrate sidewall surface of the substrate proximate to the first junction region, and depositing silicon alloy material in the second junction region superjacent to a second substrate sidewall surface of the substrate proximate to the second junction region.

21. The method of claim 17, further comprising doping the substrate material with one of phosphorous, arsenic, and antimony to form an N-type channel/well material having an electrically negative charge.

22. The method of claim 17, further comprising doping the silicon alloy material with one of boron and aluminum to form a P-type junction region material having an electrically positive charge.

23. The method of claim 17, further comprising forming a layer of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode.

24. The method of claim 23, further comprising forming a sufficient layer of conformal etch stop material on the layer of silicide material to cause a tensile strain in the channel.